EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp .
L1	1	10/630969	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/13 12:12
L3	11147	438/240,216,287,585-591,591, 770-778.CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR .	ON	2007/02/13 12:21
L4	3125	3 and chamber	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/13 12:22
L5	142	4 and first adj oxide	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON .	2007/02/13 12:22
L6	101	5 and second adj oxide	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/13 12:23
L7	0	(semiconductor ADJ microstructure ADJ positioning AND initial ADJ dielectric ADJ layer AND process ADJ chamber AND flowing WITH gas WITH oxygen ADJ gas AND chambe AND oxide ADJ layer WITH high ADJ thickness ADJ uniformity WITH oxide AND self ADJ limiting WITH oxidation ADJ process AND partial ADJ pressure oxygen ADJ containing WITH chamber WITH less ADJ than AND "50" ADJ Torr AND first AND second AND oxide).CLM.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/13 13:01

Ref #	Hits	Search Query	DBs	Default Operat or	Plural s	Time Stamp
L2	50	self near3 limiting near3 (oxidizing oxidation oxidized oxidization) with oxide	US-PGPU B; USPAT; EPO; JPO	OR	ON	2006/01/25 06:35
L3	61	self near3 limiting near5 (oxidizing oxidation oxidized oxidization) with oxide	US-PGPU B; USPAT; EPO; JPO	OR	ON	2006/01/25 06:35
L4	66	self near3 limiting near6 (oxidizing oxidation oxidized oxidization) with oxide	US-PGPU B; USPAT; EPO; JPO	OR	ON	2006/01/25 06:35
L5	95	self near3 limiting with (oxidizing oxidation oxidized oxidization) with oxide	US-PGPU B; USPAT; EPO; JPO	OR	ON	2006/01/25 06:36
L6	95	self with limiting with (oxidizing oxidation oxidized oxidization) with oxide	US-PGPU B; USPAT; EPO; JPO	OR	ON	2006/01/25 06:36
S58	1	10/630969	US-PGPU B; USPAT; EPO; JPO	OR	ON	2006/01/24 17:16
S59	7144	oxide with low adj pressure	US-PGPU B; USPAT; EPO; JPO	OR	ON	2006/01/24 17:17
S60	476	S59 and (oxide low adj pressure) with torr	US-PGPU B; USPAT; EPO; JPO	OR	ON	2006/01/24 17:17
S61	478	S59 and (oxide low adj pressure) with (torr pascal)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2006/01/24 17:18
S62	479	S59 and (oxide low adj pressure) with (torr pascal atmosphereic)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2006/01/24 17:18

S63	370	S62 and (oxide with (thick thickness thicker))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2006/01/24 17:19
S64	146	S63 and ((oxide thick thickness thicker) with angstrom)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2006/01/24 17:20
S65	74	S64 and (oxide with (oxygen 'o2' oxygen adj containing))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2006/01/24 17:24
S66	206	oxide with self adj limiting near3 oxid\$4	US-PGPU B; USPAT; EPO; JPO	OR	ON	2006/01/24 17:55
S67	50	oxide with self adj limiting near3 (oxidizing oxidation oxidized oxidization)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2006/01/24 17:56
S68	163	self adj limiting near3 (oxidizing oxidation oxidized oxidization)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2006/01/24 17:57
S69	50	self adj limiting near3 (oxidizing oxidation oxidized oxidization) with oxide	US-PGPU B; USPAT; EPO; JPO	OR .	ON	2006/01/25 06:35

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7 y	U	1		Docume	nt ID		Issue Dat	Påge	Tide	Current O	Current X Retrie	va
1	г	П	US	200500	59259	A	2005031	18	Interfacial oxidation process for high-k gate dielectric proce		257/E21.2	
2	c	r.	ÜŜ	2005002	26459	Α	2005020	16	Method of forming uniform ultra-thin oxynitride layers	438/786	257/E21.2	
3	c	G	US	2005002	26453	A	2005020	15	Formation of ultra-thin oxide layers by self-limiting interfac	438/778	257/E21.2	·
4	C	r.	US	2004022	29447	Α	2004111	26	Process for producing luminescent silicon nanoparticles	438/507		
5		L					2004092		Structure and method for bonding to copper interconnect st	228/220	228/215;	
6	1						2004050	L	METHOD OF FORMING A NITRIDE GATE DIELECTRI		257/E21.1	
7	c	Б	US	2003018	30556	Α	2003092	5	Corrosive-resistant coating over aluminum substrates for us	428/472.2	427/255.28	
8	J						2003032		Method of forming ultrathin oxide layer	438/770	257/E21.1	,
9	J					- (2003032		Method of improved high K dielectric - polysilicon interfac	257/310	257/309;	
10	ב	r.	US	2003004	19942	Α	2003031	9	Low temperature gate stack	438/778	257/E21.1	į
1,1	r	D	US	2003004	42526	Α	2003030	12	Method of improved high K dielectric-polysilicon interface	257/309	257/E21.0	=======================================
12	ה	Г	ÜS	2003003	32304	Α	2003021	14	Process for the electrochemical oxidation of a semiconduct	438/770	257/E21.2	
13	Г.	г	US	2001003	31562	Α	2001101	10	Method of forming ultrathin oxide layer	438/770	257/E21.1	
14	r	O	US	2001001	7421	Α	2001083	3	Semiconductor element with metal layer	257/767	257/E21.5	
15	D	ū	ŪS	6974779	B2		2005121	17	Interfacial oxidation process for high-k gate dielectric proce	438/769	438/770	
16	Г	ı	US	6863926	5 B2		2005030	5	Corrosive-resistant coating over aluminum substrates for us	427/250	427/249.15	
17万里	Г	г	US	6806145	5 B2		2004101	11	Low temperature method of forming a gate stack with a hig	438/287	257/E21.1	:
18	С	r	US	6794314	4 B2		2004092	11	Method of forming ultrathin oxide layer	438/778	257/E21.1	
19	п	c	US	6727134	4 B1		2004042	6	Method of forming a nitride gate dielectric layer for advanc	438/216	257/E21.1	:
?^	1_		71,035	* *******	י בם ל		3003020	12	Denotes for the electrochemical evidetics of a comic order,	439/770 ···	252/221.2	્ય
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20	г	Г.	US 6559069 B2	2003050 13	Process for the electrochemical oxidation of a semiconduct	438/770	257/E21.2	:.
21	Γ.	C	US 6492283 B2	2002121 11	Method of forming ultrathin oxide layer	438/770	257/E21.1	::
22	Ľ	c	US 6444592 B1	2002090 6	Interfacial oxidation process for high-k gate dielectric proce	438/770	257/E21.2	
23	C	Ľ.	US 6417564 B2	2002070 3	Semiconductor element with metal layer	257/740	257/763;	.;
24	r	Γ	US 6329722 B1	2001121 7	Bonding pads for integrated circuits having copper intercon	257/786	257/690;	3.
25	Б	C	US 6197641 BI	2001030 17	Process for fabricating vertical transistors	438/268	257/E21.4	
26	Ľ	L2	US 6165914 A	2000122 5	Method for fabricating semiconductor devices with thick hi	438/787	257/E21.2	
27	Ŀ	Б	US 6144071 A	2000110 18	Ultrathin silicon nitride containing sidewall spacers for imp	257/344	257/384;	···
28	г	п	US 6103595 A	2000081 6	Assisted local oxidation of silicon	438/431	257/E21.5	
29 🦡	C.	E.	US 6063665 A	2000051 6	Method for silicon surface control for shallow junction for	438/260	257/E21.3	
30	n	C	US 5961791 A	1999100 11	Process for fabricating a semiconductor device	204/192.1	204/192.15	
31	C	E.	US 5916378 A	1999062 10	Method of reducing metal contamination during semicondu	148/243	148/275;	
32 :	г	г	US 5804910 A	1998090 7	Field emission displays with low function emitters and met	313/310		
33	L.	ה	US 5661073 A	1997082 6	Method for forming field oxide having uniform thickness	438/431	257/E21.5	
34	t:	г	US 5589422 A	1996123 16	Controlled, gas phase process for removal of trace metal co	438/476	134/1.3;	
35	n	E.	US 5359216 A	1994102 9	DRAM process with improved polysilicon-to-polysilicon c	257/306	257/297;	
36	٦	п	US 5334281 A	1994080 7	Method of forming thin silicon mesas having uniform thick	438/404	148/DIG.5	
37	C	г	US RE34535 E	1994020 9	Floating gate memory with improved dielectric	365/185.0	257/319;	::
38	L:	П	US 5244825 A	1993091 8	DRAM process with improved poly-to-poly capacitor	438/241	257/E27.0	[:
30			LIS-6104810-A	1005041 13	Fahriantian of internal undislation for UDD () 1 - plated tealm.	420/ <u>5</u> 03	257.P21.2.	ائوسىا
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32	ר ר	US 5804910 A	1998090	7	Field emission displays with low function emitters and met	313/310		
33 :	r r	US 5661073 A	1997082	6	Method for forming field oxide having uniform thickness	438/431	257/E21.5	i
34	ר: ר	US 5589422 A	1996123	16	Controlled, gas phase process for removal of trace metal co	438/476	134/1.3;	5.
35	c c	US 5359216 A	1994102	9	DRAM process with improved polysilicon-to-polysilicon c	257/306	257/297;	
36	הה	US 5334281 A	1994080	7	Method of forming thin silicon mesas having uniform thick	438/404	148/DIG.5	:.
37	הה	US RE34535 E	1994020	9	Floating gate memory with improved dielectric	365/185.0	257/319;	
38	ב כ	US 5244825 A	1993091	8	DRAM process with improved poly-to-poly capacitor	438/241	257/E27.0	· :
39	ר כ	US 5104819 A	1992041	13	Fabrication of interpoly dieletric for EPROM-related techn	438/593	257/E21.2	
40	ה ה	US 5098192 A	1992032	10	DRAM with improved poly-to-poly capacitor	257/306	257/760;	
41	ה ה	US 4949154 A	1990081	11	Thin dielectrics over polysilicon	257/311	257/371;	:
42	c c	US 4922312 A	1990050	8	DRAM process with improved polysilicon-to-polysilicon c	257/297	257/300;	:.
43	ב ב	US 4697330 A	1987100	10	Floating gate memory process with improved dielectric	438/261	257/E21.6	
44	ГГ	US 4656729 A	1987041	11	Dual electron injection structure and process with self-limit	438/261	257/316;	:
45	ה ה	US 4613956 A	1986092	8	Floating gate memory with improved dielectric	365/185.0	257/315;	
46	P. C	US 4577390 A	1986032	11	Fabrication of polysilicon to polysilicon capacitors with a c	438/396	257/371;	į.
47	P C	US 4405659 A	1983092	9	Method for producing columnar grain ceramic thermal barri	427/248.1	427/250;	
48	P	US 4401697 A	1983083	10	Method for producing columnar grain ceramic thermal barri	427/250	204/192.15	3
49	e c	US 4321311 A	1982032	9	Columnar grain ceramic thermal barrier coatings	428/623	428/629;	**************************************
50	P.C	WO 2005013348 A	2005021		FORMATION OF ULTRA-THIN OXIDE AND OXYNITRI		257/E21.2	
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